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### A DEDICATED MICROPROCESSOR FOR EXTERNALLY POWERED IMPLANTABLE PAIN CONTROLLER

M Wei, J Mouine, R Fontaine, F Duval - Engineering in Medicine and Biology Society, 1995. IEEE 17th ..., 1995 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... level. The resulting schematic or netlist is then automatically placed and routed with **Cadence Preview** Cell Ensemble. OUTPUT STAGE ...

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### Castor 1.0, a VLSI analog-digital circuit for pixel imaging applications

C Colledani, G Comes, W Dulinski, Y Hu, F Loddo, R ... - Nuclear Instruments and Methods in Physics Research Section ..., 1997 - [liquids.deas.harvard.edu](http://liquids.deas.harvard.edu)

... power supply line resistances. The layout of the digital part was done in **Preview**, the **Cadence** automatic routing package. A top-down strategy was adopted. ...

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### A flexible SRAM Compiler for embedded application

Y Liu, Z Gao - Solid-State and Integrated-Circuit Technology, 2001. ..., 2001 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... By means of **Preview** and Silicon Ensemble in **Cadence**, the SEAM Compiler presents the Abstract model for automatic layout and route. ...

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### A Design Methodology for Hardware Prototyping of Integrated AC Drive Control: Application to Direct ...

P Poure, F Aubert, F Braun - PROC INT WORKSHOP RAPID SYST PROTOTYPING. pp. 90-95. 2000, 2000 - [doi.ieeeecs.org](http://doi.ieeeecs.org)

... compiler IC **Preview** tools (**Cadence** environment) Leapfrog digital simulator & SpectreS analog simulator (**Cadence** environment) MAX ...

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### A graph-partitioning-based approach for multi-layer constrained via minimization

YC Chou, YL Lin - Proceedings of the 1998 IEEE/ACM international conference on ..., 1998 - [portal.acm.org](http://portal.acm.org)

... 14 **CADENCE**, **Preview** Cell Ensemble Reference Manual, Version 4.2.1, Sep. 1992. 15

EDIF Schematic Technical Subcommittee, EDIF ~ 0 0 User Guide, Sep. 1987. ...

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### Logic Depth and Power Consumption: A comparative Study Between Standard Cells and FPGAs

E Boemo, S Lopez-Buedo, CS Perez, J Jauregui, J ... - Proceedings of the XIII Design of Circuits and Integrated ..., 1998 - [ii.uam.es](http://ii.uam.es)

... IEEE Trans. on Computers, pp.945-951, July 1990. [15] **Cadence**, "**Preview** Cell Ensemble. Reference Manual". **Cadence** 1992. [16] T ...

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### generators 8%.

MS Anderson, S Summerfield - ELECTRONICS LETTERS, 1996 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... Relative VLSI cost: The above designs were implemented in ES2 1 pn standard cell CMOS technology using the **Preview** Place and Route tools in **Cadence** DFWII, with ...

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### Relative VLSI costs of WDFs implemented using redundant and non-redundant arithmetic

MS Anderson, S Summerfield - Electronics Letters, 1996 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... Relative VLSI cost: The above designs were implemented in ES2 1 pn standard cell CMOS technology using the **Preview** Place and Route tools in **Cadence** DFWII, with ...

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### Logical-Physical Co-design for Deep Submicron Circuits: Challenges and Solutions

M Pedram - Proc. Asia and South Pacific Design Automation Conf, 1998 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... Examples of commercial RT-level floorplan- ners are **Preview[tm]** from **Cadence** and Planet-PL[tm] from Avant!. I. LAYOUT-DRIVEN LOGIC SYNTHESIS ...

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### A New Methodology for Using Orcad Applications on a Network

L Viman, G Chindris, O Pop - Electronics Technology: Concurrent Engineering in Electronic ..., 2001 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

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